AMENDMENTS TO THE CLAIMS

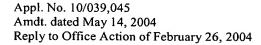The listing of claims below replaces all prior versions, and listings, of claims:

1   1.   (Original) A method of controlling access to a shared memory of a multiprocessor

2   system, the multiprocessor system comprising a first bus and a second bus coupled to the

3   shared memory, the first bus coupled to a first processor, and the second bus coupled to a

4   second processor, the method comprising the steps of:

5   requesting exclusive access to a first memory location of the shared memory by

6   the first processor;

7   granting exclusive access to the first memory location of the shared memory to

8   the first processor; and

9   allowing access to a second memory location of the shared memory to the second

10   processor while the first processor has exclusive access to the first memory location.

1   2.   (Original) The method of claim 1, the step of requesting exclusive access

2   comprising the steps of:

3   asserting a lock signal on the first bus; and

4   sending a lock request from the first processor to a memory controller coupled to

5   the first bus, the second bus, and the shared memory.

1   3.   (Original) The method of claim 2, the step of asserting a lock signal further

2   comprising the step of:

3   asserting a split lock signal on the first bus, the split lock signal indicating that the

4   lock request contains two memory address data.

1   4.   (Original) The method of claim 2, the step of requesting exclusive access further

2   comprising the step of:

3   forwarding the lock request from the memory controller to a switch; and

4   signaling the first processor to retry the lock request.

1   5.   (Original) The method of claim 4, the step of granting exclusive access

2   comprising the steps of:

3   signaling the memory controller by the switch to retry the lock request;

4   assigning exclusive access to the first memory location by the switch;

5   notifying the memory controller of the exclusive access assigned in the assigning

6   step; and

7   granting exclusive access to the first memory location by the memory controller

8   responsive to a retry of the lock request by the first processor.

1   6.   (Original) The method of claim 5, the step of assigning exclusive access to the

2   memory location by the switch comprising the steps of:

3   determining if the first memory location is currently assigned;

4   saving a lock request information if the first memory locations is not currently

5   assigned; and

6   sending the lock request information to the memory controller.

1   7.   (Original) The method of claim 6, the lock request information comprising:

2   a node ID of the first processor;

3   a cycle ID of the first processor; and

4   memory address data for a first memory location.

1   8.   (Original) The method of claim 7, the memory address data comprising:

2   a first memory address; and

3   a second memory address,

4   wherein the first memory address can be non-contiguous with the second memory

5   address.

1   9.   (Original) The method of claim 1, further comprising the step of:

2   releasing exclusive access to the first memory location.

1   10.   (Original) A method of controlling access to memory of a multinodal computer

2   system, the multinodal computer system comprising a plurality of multiprocessor nodes,

3   the method comprising the steps of:

4   requesting exclusive access to a first memory location of a shared memory by a

5   first processor of a first multiprocessor node the plurality of multiprocessor nodes;

6   granting exclusive access to the first memory location of the shared memory to

7   the first processor; and

8   allowing access to a second memory location of the shared memory to a second

9   processor of a second multiprocessor node of the plurality of multiprocessor nodes while

10   the first processor has exclusive access to the first memory location.

1   11.   (Original) The method of claim 10, the requesting step comprising:

2   asserting a lock signal on a first bus, the first bus coupling the first processor and

3   a first memory controller of the first multiprocessor node; and

4   sending a lock request to the first memory controller;

5   forwarding the lock request from the first memory controller to a switch, the

6   switch coupled to each of the plurality of multiprocessor nodes.

1   12.   (Currently Amended) The method of claim 10, the shared memory comprising:

2   a first memory coupled to the first memory controller; and

3   a second memory coupled to a second memory controller of a different

4   multiprocessor node of the plurality of multiprocessor nodes;.

1   13.   (Original) The method of claim 12, the step of asserting a lock signal comprising

2   the step of:

3   asserting a split lock signal on the first bus, the split lock signal indicating that the

4   lock request contains a first memory address data and a second memory address data.

1   14.   (Original) The method of claim 13, the first memory address data referencing the

2   first memory and the second memory address data referencing the second memory.

1   15.   (Original) The method of claim 13, the first memory address data referencing the

2   second memory and the second memory address data referencing the first memory.

1   16.   (Currently Amended) The method of claim 10, the step of requesting exclusive

2   access further comprising the step of:

3   forwarding the lock request form the first memory controller to the switch; and

4   signaling the first processor to retry the lock request.

1   17.   (Original) The method of claim 10, the step of granting exclusive access

2   comprising the steps of:

3   signaling the first memory controller to retry the lock request;

4   assigning exclusive access to the memory location by the switch;

5   notifying the memory controller of the exclusive access assigned in the assigning

6   step; and

7   assigning exclusive access to the first memory location by the first memory

8   controller responsive to a retry of the lock request by the first processor.

1   18.   (Original) The method of claim 17, the step of assigning exclusive access to the

2   memory location by the switch comprising the steps of:

3   determining if the first memory location is currently assigned;

4   saving a lock request information if the first memory location is not current

5   assigned; and

6   broadcasting the lock request information to each memory controller of each of

7   the plurality of multiprocessor nodes.

1   19.   (Original) The method of claim 18, the lock request information comprising:

2   a node ID of the first multiprocessor node;

3   a cycle ID of the first processor; and

4   a memory address data for the first memory location.

1   20.   (Original) The method of claim 10, further comprising the step of:

2   releasing exclusive access to the first memory location.

1   21.   (Currently Amended) A computer system for utilizing a shared memory, the

2   computer system comprising:

3   a first multiprocessor node, comprising:

4   a first process bus;

5   a first processor, coupled to the first processor bus, the first processor

6   comprising:

7   circuitry to generate an exclusive access request for a first memory

8   location ~~to the first memory controller~~;

9   a second processor bus;

10   a second processor, coupled to the second processor bus, the second processor

11   adapted to ~~perform the step of~~:

12   ~~requesting~~ request access to a second memory location;

13   a first memory;

14   a first memory controller, coupled to the first processor bus, the second processor

15   bus, and the first memory, the first memory controller adapted to ~~perform the steps of~~:

16   ~~allowing~~ allow exclusive access to the first memory location by the first

17   processor; and

18   ~~allowing~~ allow access to the second memory location by the second

19   processor while the first processor has exclusive access to the first memory location.

1   22.   (Currently Amended) The computer system of claim 21, further comprising:

2   a second multiprocessor node, comprising:

3   a third process bus;

4   a third processor, coupled to the third processor bus, the third processor

5   adapted to ~~perform the executable step of~~:

6   ~~requesting~~ request access to a third memory location;

7   a second memory;

8   a second memory controller, coupled to the third processor bus, and the

9   first memory, the second memory controller adapted to ~~perform the steps of~~:

10   ~~allowing~~ allow exclusive access to the first memory location by the

11   first processor;

12   ~~allowing~~ allow access to the second memory location by the

13   second processor while the first processor has exclusive access to the first memory

14   location; and

15   ~~allowing~~ allow access to the third memory location by the third

16   processor while the first processor has exclusive access to the first memory location; and

17   a switch, coupled to the first memory controller and the second memory

18   controller, for switching transactions between the first multiprocessor node and the

19   second multiprocessor node.

1   23.   (Original) The computer system of claim 22, the first memory location

2   comprising:

3   a first portion in the first memory; and

4   a second portion in the second memory.

1   24.   (Original) The computer system of claim 22,

2   wherein the first memory location is in the first memory, and

3   wherein the second memory location is in the first memory.

1   25.   (Original) The computer system of claim 22,

2   wherein the first memory location is in the first memory, and

3   wherein the third memory location is in the first memory.

1   26.   (Original) The computer system of claim 22,

2   wherein the first memory location is in the second memory, and

3   wherein the third memory location is in the second memory.

1   27.   (Original) The computer system of claim 22,

2   wherein the first memory location is in the second memory, and

3   wherein the third memory location is in the first memory.

7

1   28.   (Original) The computer system of claim 22, the switch comprising:

2   a lock register for storing a lock control information.

1   29.   (Original) The computer system of claim 28, the lock control information

2   comprising:

3   a node ID corresponding to the first processor;

4   a cycle ID corresponding to the first processor; and

5   a first memory address corresponding to the first memory location.

1   30.   The computer system of claim 29, the lock control information further

2   comprising:

3   a second memory address corresponding to the first memory location.

1   31.   (Currently Amended) The computer system of claim 29, the switch comprising:

2   circuitry to signal the first memory controller to retry the step of allowing

3   exclusive access to the first memory location by the first processor;

4   ·   circuitry to arbitrate among requests for exclusive access to the first memory

5   location;

6   circuitry to broadcast the lock control information to the first memory controller

7   and the second memory controller.

1   32.   (Original) The computer system of claim 31, the first memory controller further

2   comprising:

3   circuitry to signal the first processor to retry the exclusive access request;

4   circuitry to shadow the lock control information broadcast by the switch; and

5   the second memory controller further comprising:

6   circuitry to shadow the lock control information broadcast by the switch.

1 33.   (Original) The computer system of claim 30, wherein the first memory address

2 can be in either the first memory or the second memory, and

3   wherein the second memory address can be in either the first memory or the

4 second memory.

1 34.   (New) The method of claim 1, wherein requesting exclusive access comprises:

2   sending a lock request from the first processor to a first memory controller

3 coupled to the shared memory;

4   forwarding the lock request from the memory controller to a switch; and

5   the switch broadcasting lock request information to the first memory controller

6 and at least another memory controller.

1 35.   (New) The method of claim 34, further comprising:

2   each of the first memory controller and at least another memory controller storing

3 the lock request information.

1 36.   (New) The method of claim 35, further comprising the switch storing the lock

2 request information in a register in the switch,

3   wherein the memory controllers also store the switch request information in

4 respective registers in the memory controllers.

9